

# IS62WV12816DALL/DBLL IS65WV12816DALL/DBLL



## 128K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

SEPTEMBER 2011

### FEATURES

- High-speed access time: 35ns, 45ns, 55ns
- CMOS low power operation
  - 36 mW (typical) operating
  - 9  $\mu$ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  - 1.8V  $\pm$  10%  $V_{DD}$  (IS62/65WV12816DALL)
  - 2.5V--3.6V  $V_{DD}$  (IS62/65WV12816DBLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial and Autotmovie temperature support
- 2CS Option Available
- Lead-free available

### DESCRIPTION

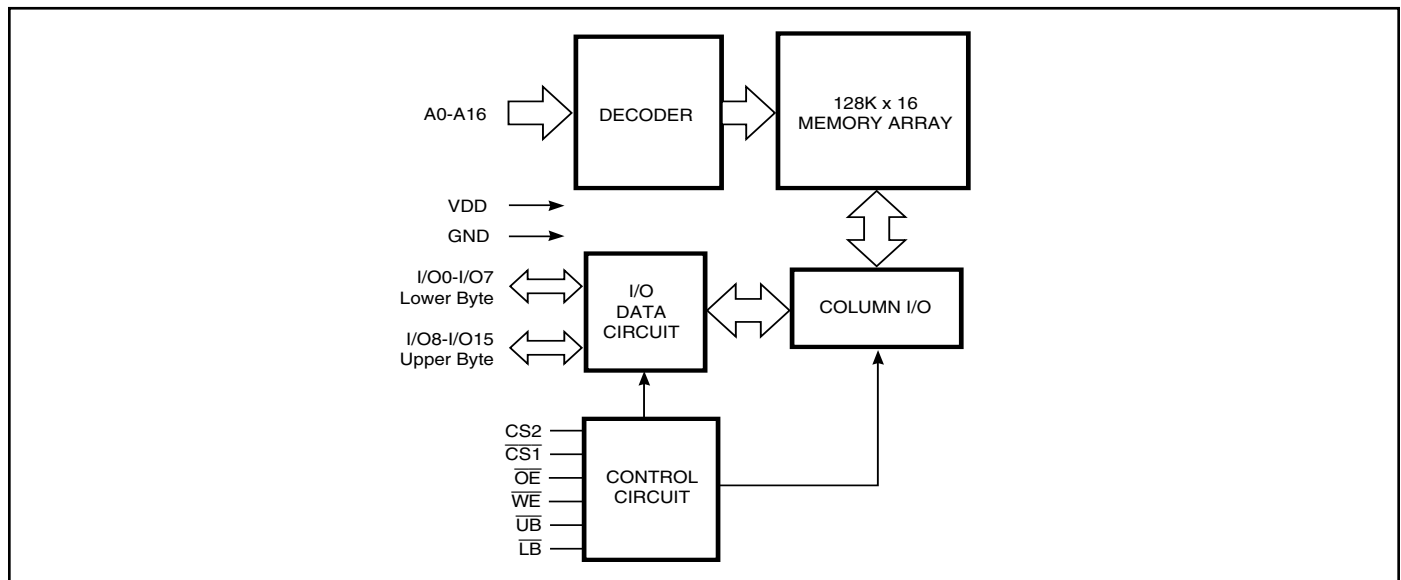
The *ISSI* IS62/65WV12816DALL/DBLL are high-speed, 2M bit static RAMs organized as 128K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When  $\overline{CS1}$  is HIGH (deselected) or when  $\overline{CS2}$  is LOW (deselected) or when  $\overline{CS1}$  is LOW,  $\overline{CS2}$  is HIGH and both  $\overline{LB}$  and  $\overline{UB}$  are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory. A data byte allows Upper Byte ( $\overline{UB}$ ) and Lower Byte ( $\overline{LB}$ ) access.

The IS62/65WV12816DALL/DBLL are packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm) and 44-Pin TSOP (TYPE II).

### FUNCTIONAL BLOCK DIAGRAM



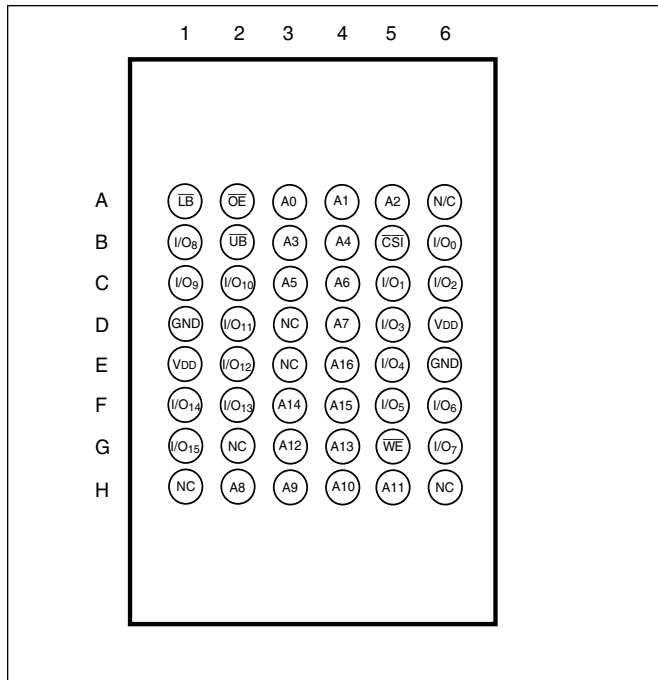
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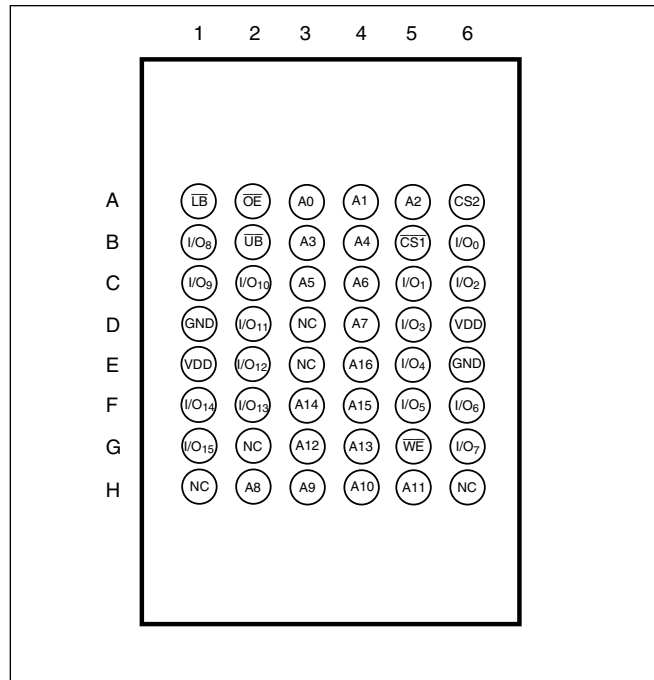
- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

**PIN CONFIGURATIONS**

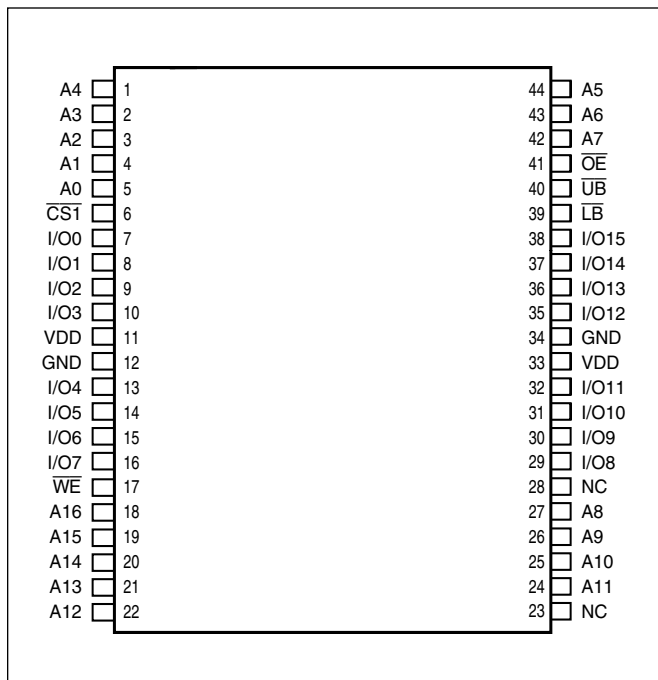
**48-Pin mini BGA (6mm x 8mm)  
(Package Code B)**



**48-Pin mini BGA (6mm x 8mm)  
2 CS Option (Package Code B2)**



**44-Pin mini TSOP (Type II)  
(Package Code T)**



**PIN DESCRIPTIONS**

A0-A16	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CS1, CS2	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
LB	Lower-byte Control (I/O0-I/O7)
UB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground



**TRUTH TABLE**

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN		V <sub>DD</sub> Current
							I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	X	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
	X	X	L	X	X	X	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
	X	X	X	X	H	H	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I <sub>CC</sub>
	H	L	H	H	X	L	High-Z	High-Z	I <sub>CC</sub>
Read	H	L	H	L	L	H	DOUT	High-Z	I <sub>CC</sub>
	H	L	H	L	H	L	High-Z	DOUT	
	H	L	H	L	L	L	DOUT	DOUT	
Write	L	L	H	X	L	H	D <sub>IN</sub>	High-Z	I <sub>CC</sub>
	L	L	H	X	H	L	High-Z	D <sub>IN</sub>	
	L	L	H	X	L	L	D <sub>IN</sub>	D <sub>IN</sub>	

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.2 to V <sub>DD</sub> +0.3	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

**Note:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING RANGE (V<sub>DD</sub>)**

Range	Ambient Temperature	IS62WV12816DALL	IS62WV12816DBLL
Commercial	0°C to +70°C	1.8V ± 10%	2.5V - 3.6V
Industrial	-40°C to +85°C	1.8V ± 10%	2.5V - 3.6V
		IS65WV12816DALL	IS65WV12816DBLL
Automotive	-40°C to +125°C	1.8V ± 10%	2.5V - 3.6V

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

Symbol	Parameter	Test Conditions	V <sub>DD</sub>	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	1.8V ± 10%	1.4	—	V
		I <sub>OH</sub> = -1 mA	2.5-3.6V	2.2	—	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	1.8V ± 10%	—	0.2	V
		I <sub>OL</sub> = 2.1 mA	2.5-3.6V	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		1.8V ± 10%	1.4	V <sub>DD</sub> + 0.2	V
			2.5-3.6V	2.2	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		1.8V ± 10%	-0.2	0.4	V
			2.5-3.6V	-0.2	0.6	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>		-1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled		-1	1	μA

**Notes:**

For IS62/65WV12816DALL:

V<sub>IL</sub> (min.) = -1.0V AC (pluse width < 10ns). Not 100% tested.

V<sub>IH</sub> (max.) = V<sub>DD</sub> + 1.0V AC; (pluse width < 10ns). Not 100% tested.

For IS62/65WV12816DBLL:

V<sub>IL</sub> (min.) = -2.0V AC (pluse width < 10ns). Not 100% tested.

V<sub>IH</sub> (max.) = V<sub>DD</sub> + 2.0V AC; (pluse width < 10ns). Not 100% tested.

**CAPACITANCE**<sup>(1)</sup>

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	10	pF

**Note:**

1. Tested initially and after any design or process changes that may affect these parameters.

# IS62WV12816DALL/DBLL, IS65WV12816DALL/DBLL

## IS62/65WV12816DALL, POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 55	Unit
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	15	mA
			Ind.	20	
			Auto.	25	
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = 0	Com.	3	mA
			Ind.	3	
			Auto.	4	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IH}$ , CS2 = V <sub>IL</sub> , f = 1 MHz	Com.	0.3	mA
			Ind.	0.3	
			Auto.	0.5	
	ULB Control	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IL}$ , f = 0, $\overline{UB} = V_{IH}$ , $\overline{LB} = V_{IH}$	<b>OR</b>		
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., $\overline{CS1} \geq V_{DD} - 0.2V$ , CS2 ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com.	4	μA
			Ind.	6	
			Auto.	15	
	ULB Control	V <sub>DD</sub> = Max., $\overline{CS1} = V_{IL}$ , CS2 = V <sub>IH</sub> V <sub>IN</sub> ≤ 0.2V, f = 0; $\overline{UB} / \overline{LB} = V_{DD} - 0.2V$	<b>OR</b>		

## IS62/65WV12816DBLL, POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions		Max 35	Max. 45	Max. 55	Unit
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	22	20	18	mA
			Ind.	23	21	19	
			Auto.	35	30	25	
			typ. <sup>(2)</sup>	15	12	10	
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = 0	Com.	3	3	3	mA
			Ind.	3	3	3	
			Auto.	4	4	4	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IH}$ , CS2 = V <sub>IL</sub> , f = 1 MHz	Com.	0.1	0.1	0.1	mA
			Ind.	0.1	0.1	0.1	
			Auto.	0.2	0.2	0.2	
	ULB Control	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IL}$ , f = 0, $\overline{UB} = V_{IH}$ , $\overline{LB} = V_{IH}$	<b>OR</b>				
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., $\overline{CS1} \geq V_{DD} - 0.2V$ , CS2 ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com.	5	5	5	μA
			Ind.	7	7	7	
			Auto.	15	15	15	
	ULB Control	V <sub>DD</sub> = Max., $\overline{CS1} = V_{IL}$ , CS2 = V <sub>IH</sub> V <sub>IN</sub> ≤ 0.2V, f = 0; $\overline{UB} / \overline{LB} = V_{DD} - 0.2V$	<b>OR</b>				

### Note:

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

**AC TEST CONDITIONS**

Parameter	IS62/65WV12816DALL (Unit)	IS62/65WV12816DBLL (Unit)
Input Pulse Level	0.4V to $V_{DD}-0.2V$	0.4V to $V_{DD}-0.3V$
Input Rise and Fall Times	1V/1ns	1V/1ns
Input and Output Timing and Reference Level	$V_{REF}$	$V_{REF}$
Output Load	See Figures 1 and 2	See Figures 1 and 2

	1.8V ± 10%	2.5V - 3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
$V_{REF}$	0.9V	1.5V
$V_{TM}$	1.8V	2.8V

**AC TEST LOADS**

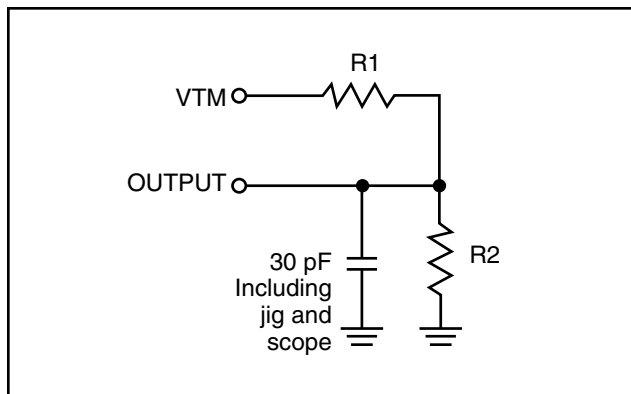


Figure 1

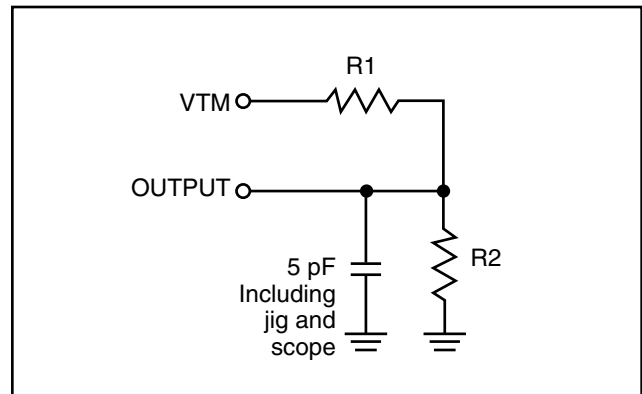


Figure 2

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

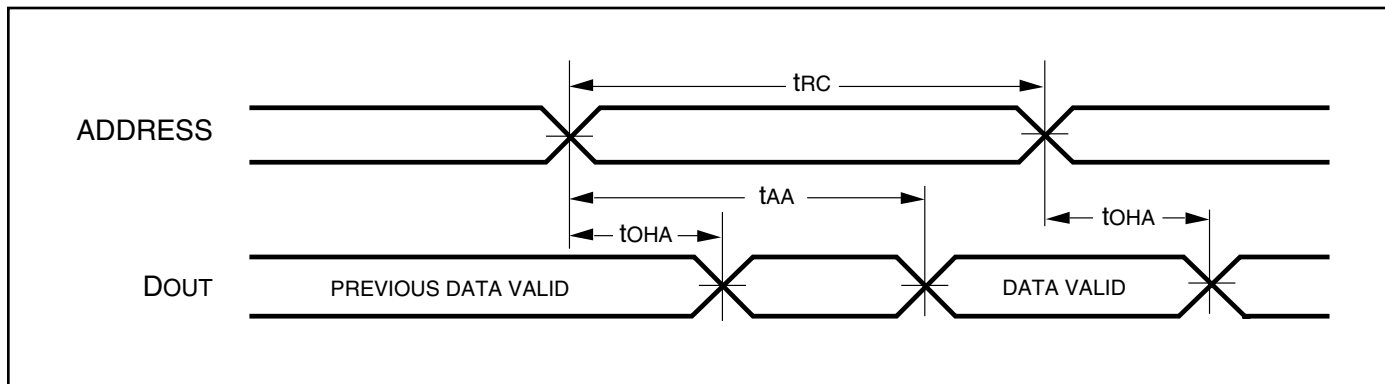
Symbol	Parameter	35 ns		45 ns		55 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	35	—	45	—	55	—	ns
t <sub>AA</sub>	Address Access Time	—	35	—	45	—	55	ns
t <sub>OHA</sub>	Output Hold Time	10	—	10	—	10	—	ns
t <sub>ACS1</sub> /t <sub>ACS2</sub>	$\overline{\text{CS1}}/\overline{\text{CS2}}$ Access Time	—	35	—	45	—	55	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ Access Time	—	15	—	20	—	25	ns
t <sub>HZOE</sub> <sup>(2)</sup>	$\overline{\text{OE}}$ to High-Z Output	—	10	—	15	—	20	ns
t <sub>LZOE</sub> <sup>(2)</sup>	$\overline{\text{OE}}$ to Low-Z Output	5	—	5	—	5	—	ns
t <sub>HZCS1</sub> /t <sub>HZCS2</sub> <sup>(2)</sup>	$\overline{\text{CS1}}/\overline{\text{CS2}}$ to High-Z Output	0	10	0	15	0	20	ns
t <sub>LZCS1</sub> /t <sub>LZCS2</sub> <sup>(2)</sup>	$\overline{\text{CS1}}/\overline{\text{CS2}}$ to Low-Z Output	10	—	10	—	10	—	ns
t <sub>BA</sub>	$\overline{\text{LB}}, \overline{\text{UB}}$ Access Time	—	35	—	45	—	55	ns
t <sub>HZB</sub>	$\overline{\text{LB}}, \overline{\text{UB}}$ to High-Z Output	0	10	0	15	0	20	ns
t <sub>LZB</sub>	$\overline{\text{LB}}, \overline{\text{UB}}$ to Low-Z Output	0	—	0	—	0	—	ns

**Notes:**

1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

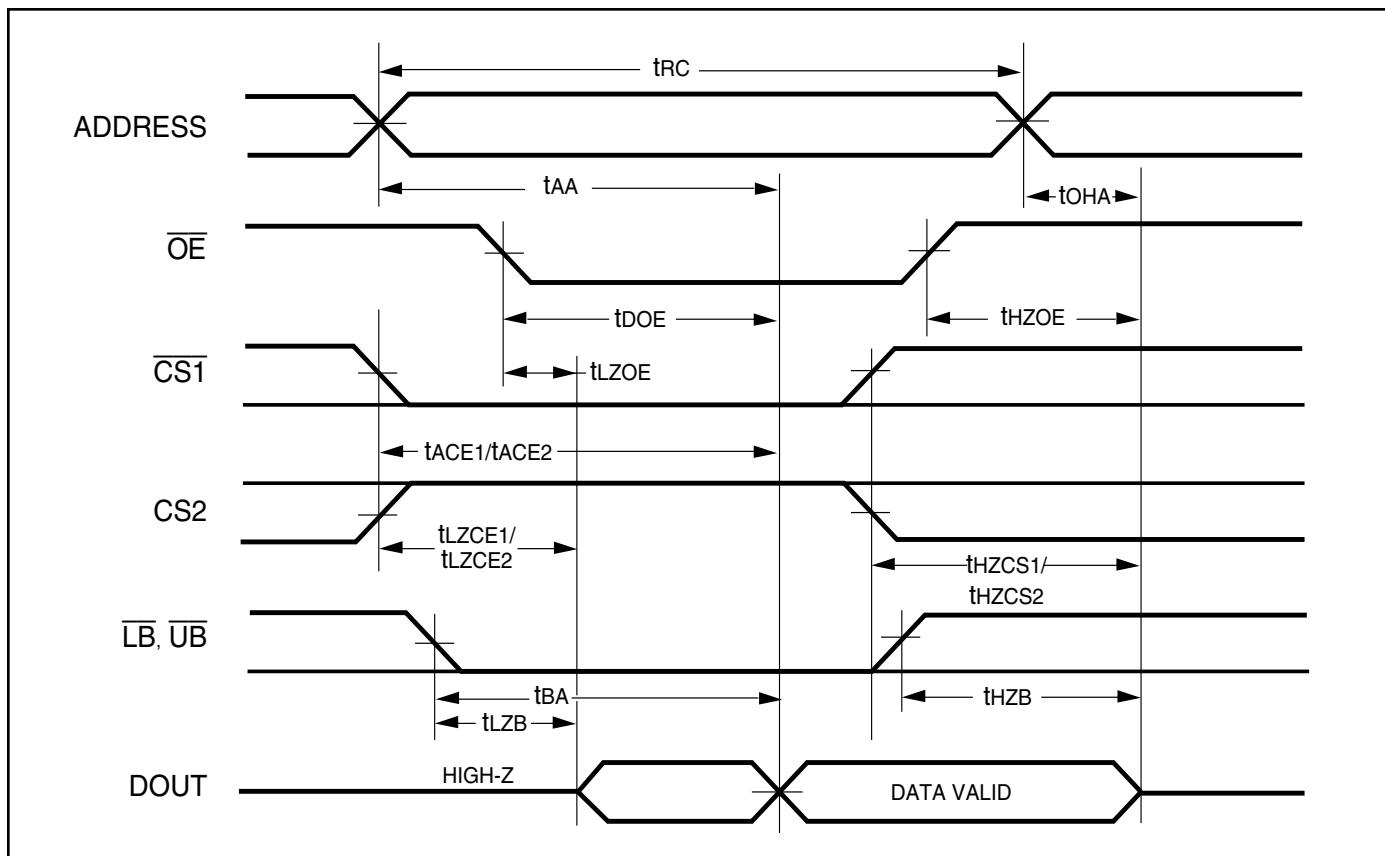
**AC WAVEFORMS**

**READ CYCLE NO. 1<sup>(1,2)</sup>** (Address Controlled) ( $\overline{CS1} = \overline{OE} = V_{IL}$ ,  $CS2 = \overline{WE} = V_{IH}$ ,  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ )



**AC WAVEFORMS**

**READ CYCLE NO. 2<sup>(1,3)</sup>** ( $\overline{CS1}$ ,  $CS2$ ,  $\overline{OE}$ , AND  $\overline{UB}/\overline{LB}$  Controlled)



**Notes:**

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CS1}$ ,  $\overline{UB}$ , or  $\overline{LB} = V_{IL}$ .  $CS2 = \overline{WE} = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CS1}$  LOW transition.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup>** (Over Operating Range)

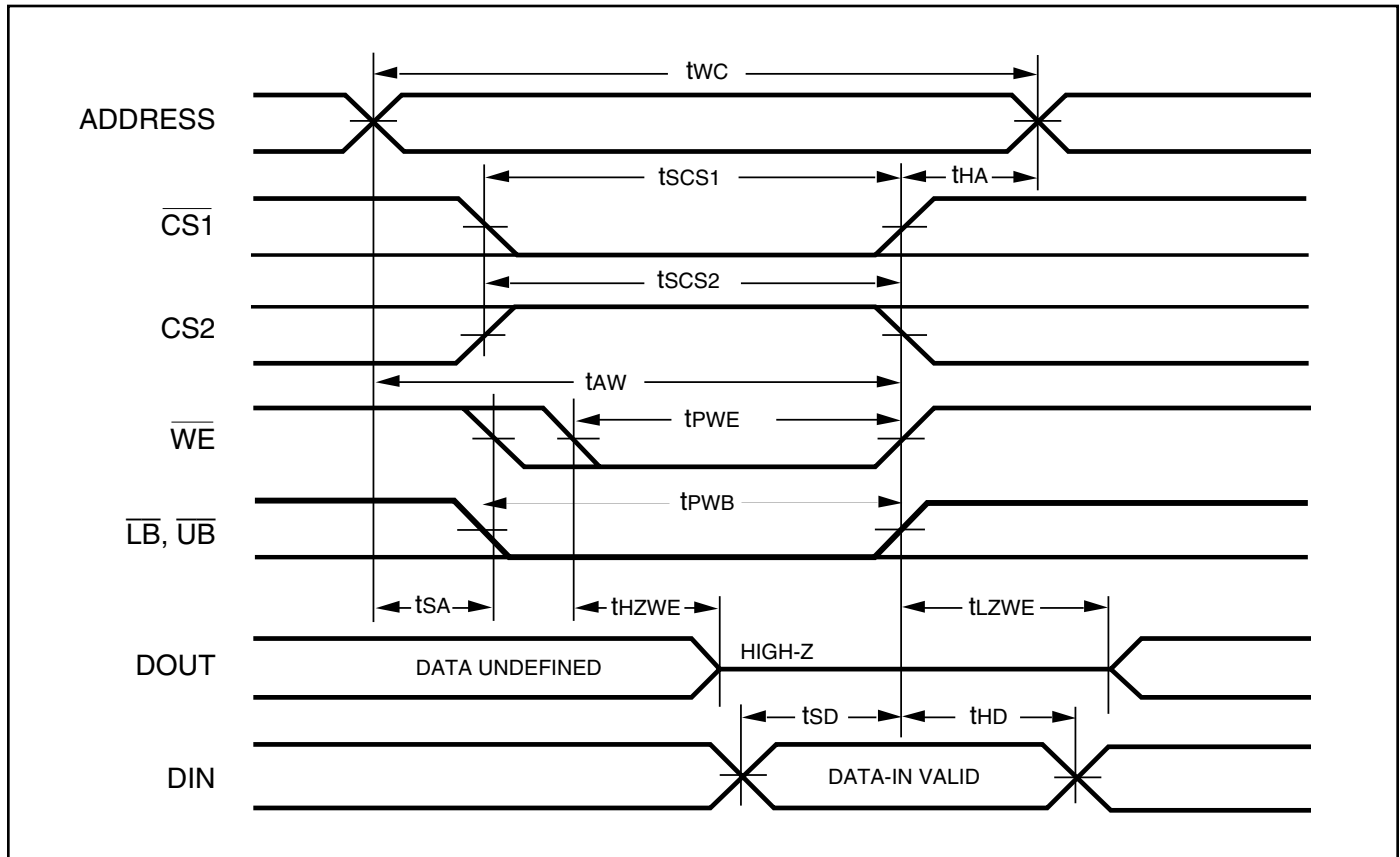
Symbol	Parameter	35 ns		45 ns		55 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	35	—	45	—	55	—	ns
t <sub>SCS1</sub> /t <sub>SCS2</sub>	$\overline{CS1}$ / $\overline{CS2}$ to Write End	25	—	35	—	45	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	25	—	35	—	45	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	0	—	ns
t <sub>PWB</sub>	$\overline{LB}$ , $\overline{UB}$ Valid to End of Write	30	—	35	—	45	—	ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	30	—	35	—	40	—	ns
t <sub>SD</sub>	Data Setup to Write End	15	—	20	—	25	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	0	—	ns
t <sub>HZWE</sub> <sup>(3)</sup>	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	—	20	ns
t <sub>LZWE</sub> <sup>(3)</sup>	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

**Notes:**

1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. The internal write time is defined by the overlap of  $\overline{CS1}$  LOW,  $\overline{CS2}$  HIGH and  $\overline{UB}$  or  $\overline{LB}$ , and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

**AC WAVEFORMS**

**WRITE CYCLE NO. 1<sup>(1,2)</sup>** ( $\overline{CS1}$  Controlled,  $\overline{OE}$  = HIGH or LOW)

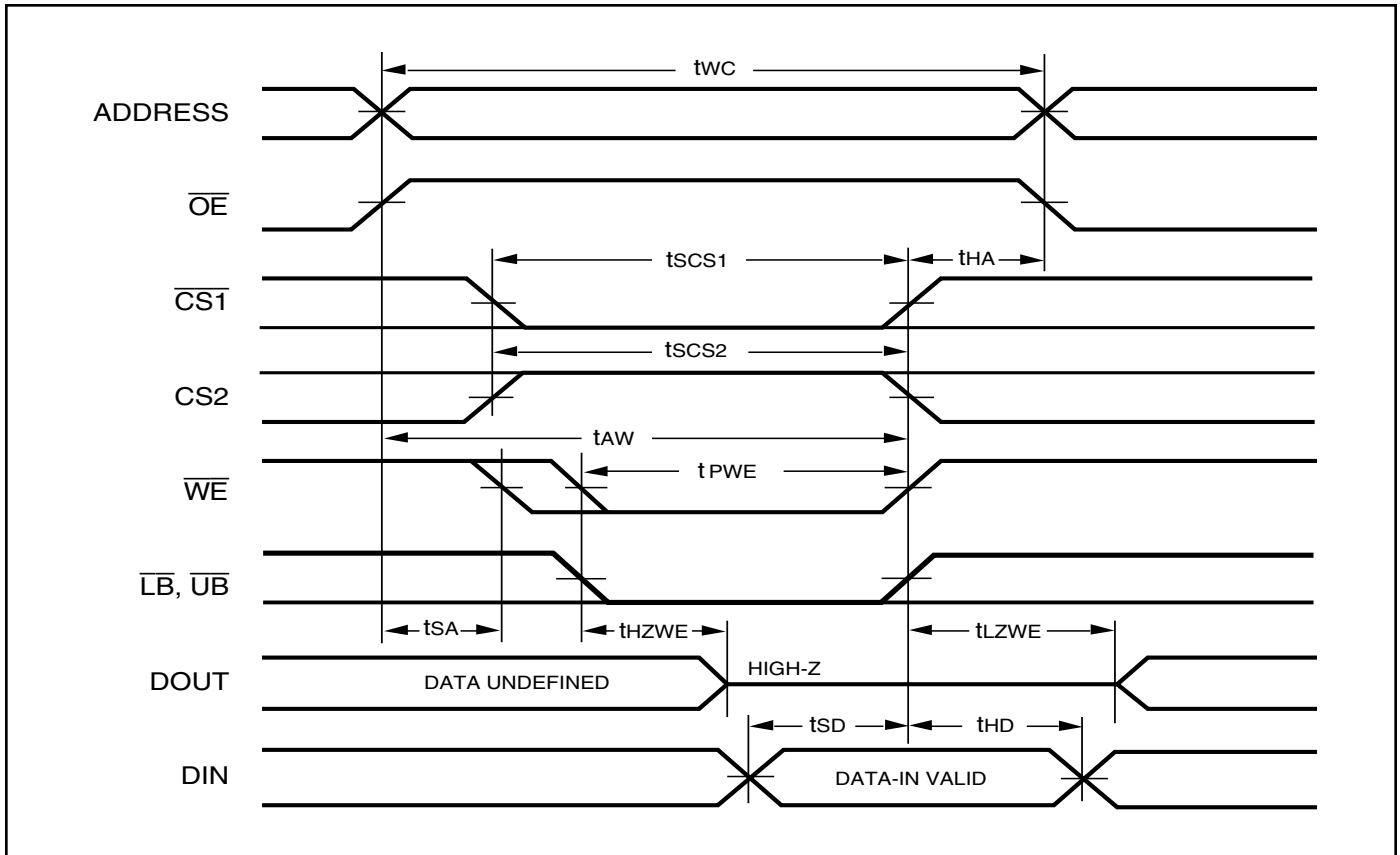


**Notes:**

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the  $\overline{CS1}$ ,  $\overline{CS2}$  and  $\overline{WE}$  inputs and at least one of the  $\overline{LB}$  and  $\overline{UB}$  inputs being in the LOW state.
2.  $WRITE = (\overline{CS1}) [ (\overline{LB}) = (\overline{UB}) ] (\overline{WE})$ .

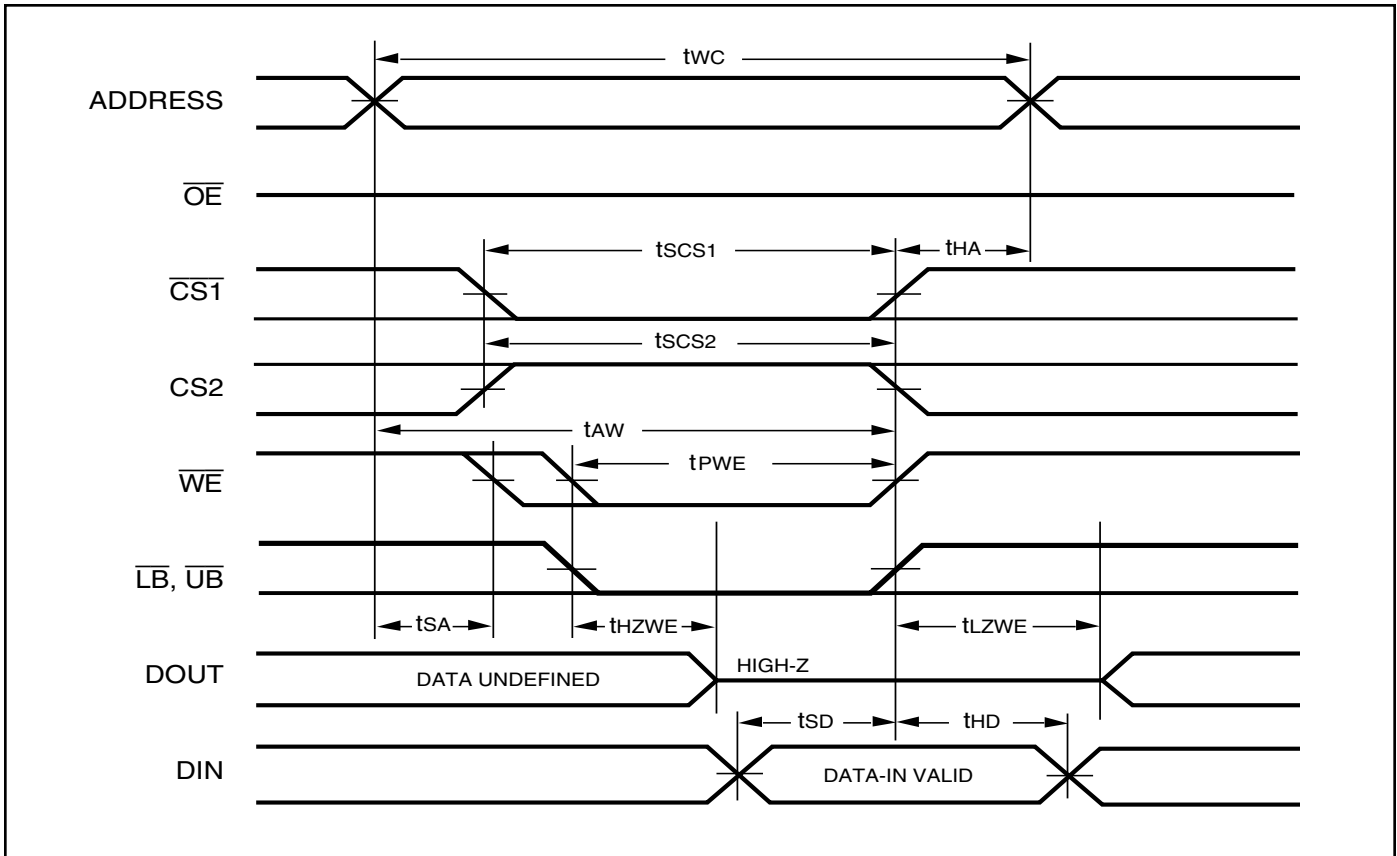
**AC WAVEFORMS**

**WRITE CYCLE NO. 2** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)



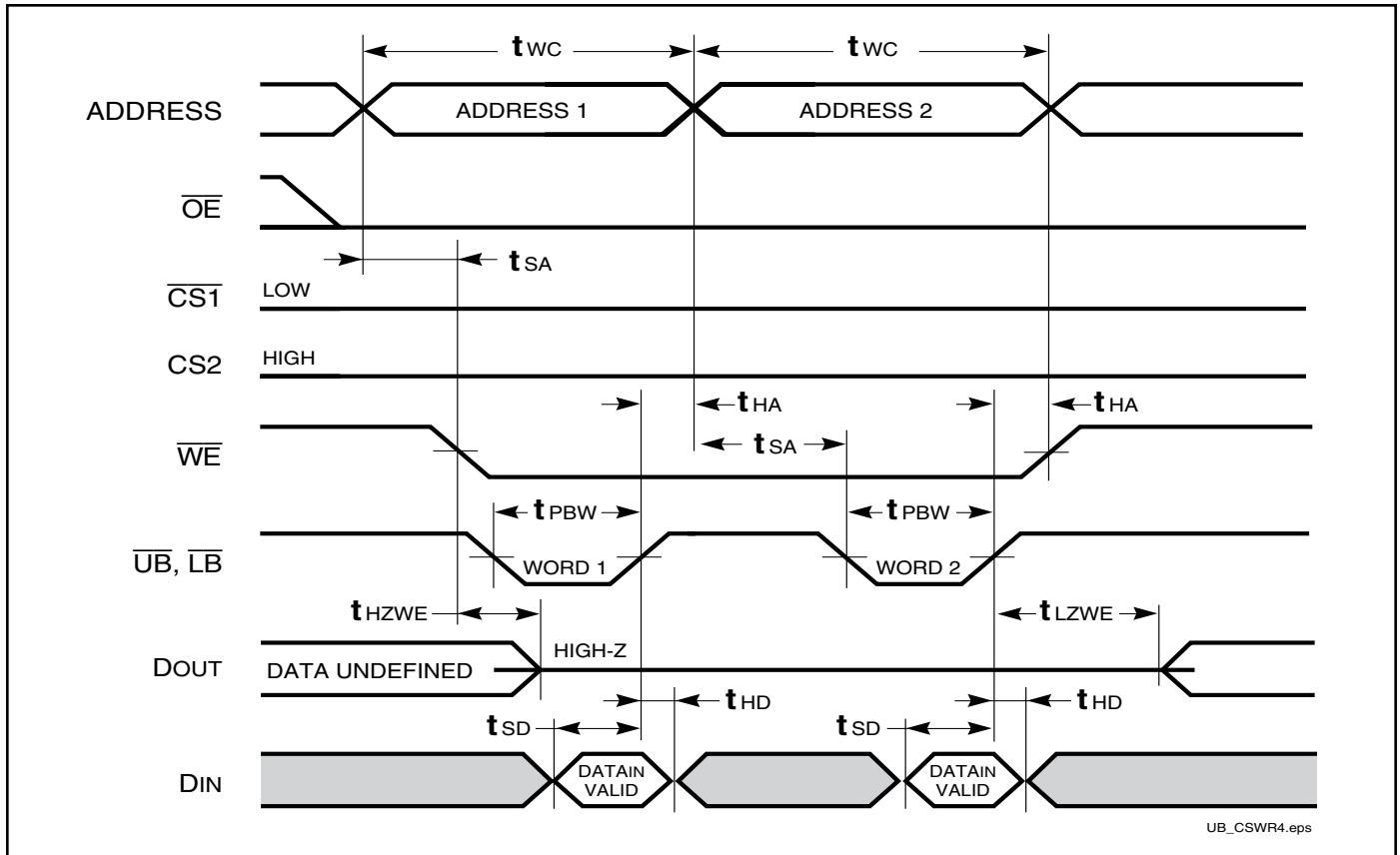
**AC WAVEFORMS**

**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)



AC WAVEFORMS

WRITE CYCLE NO. 4 ( $\overline{UB}/\overline{LB}$  Controlled)

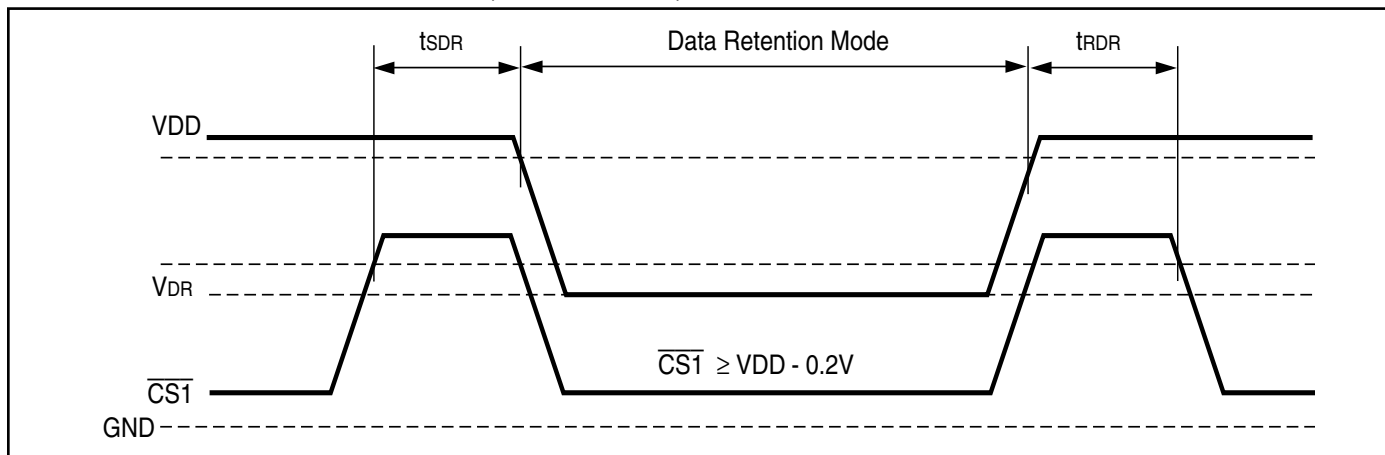


**DATA RETENTION SWITCHING CHARACTERISTICS**

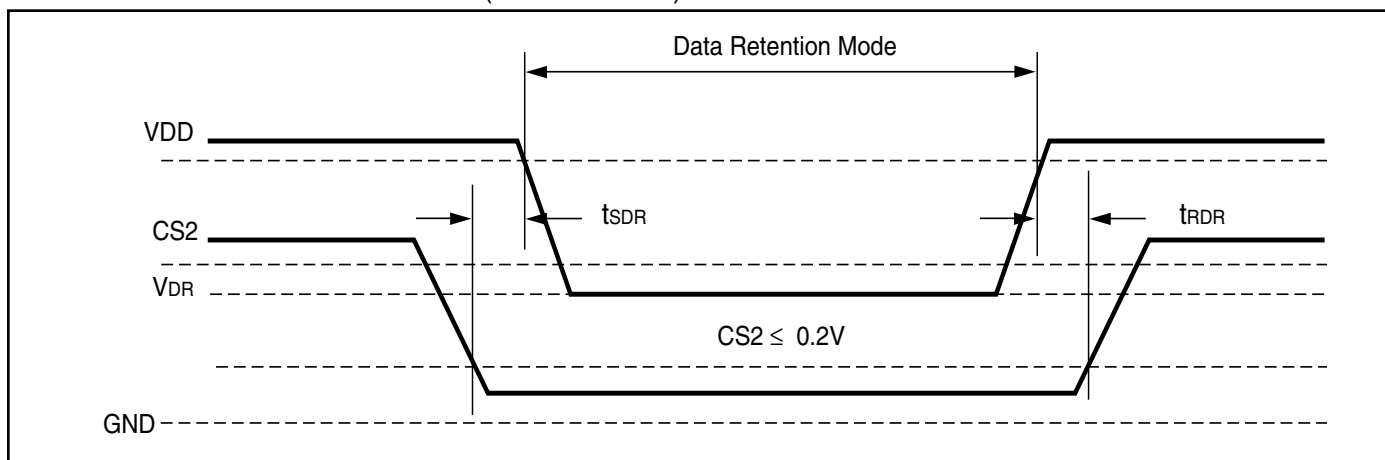
Symbol	Parameter	Test Condition	Min.	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	See Data Retention Waveform	1.5	3.6	V
I <sub>DR</sub>	Data Retention Current	V <sub>DD</sub> = 1.5V, CS1 ≥ V <sub>DD</sub> - 0.2V, CS2 ≥ V <sub>DD</sub> - 0.2V, or 0V ≤ CS2 ≤ 0.2V, 0V ≤ Vin	Com. Ind. Auto. typ. <sup>(2)</sup>	— 4 6 15 2	μA μA μA μA
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform	t <sub>RC</sub>	—	ns

- Note:**
- In data retention mode, CS2 controls the address,  $\overline{WE}$ ,  $\overline{CS1}$ ,  $\overline{OE}$ , and the Din buffer. If CS2 controls data retention mode, Vin (for these inputs) can be in the high impedance state. If  $\overline{CS1}$  controls the data retention mode, CS2 must satisfy either CS2 ≥ V<sub>CC</sub> - 0.2 V or CS2 ≤ 0.2 V. The other input levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.
  - Typical values are measured at V<sub>DD</sub> = V<sub>DR</sub>(min), T<sub>A</sub> = 25°C and not 100% tested.

**DATA RETENTION WAVEFORM (CS1 Controlled)**



**DATA RETENTION WAVEFORM (CS2 Controlled)**





**ORDERING INFORMATION: IS62WV12816DALL (1.65V - 2.2V)**

**Industrial Range: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
55	IS62WV12816DALL-55TI	TSOP (Type II)
	IS62WV12816DALL-55BI	mini BGA (6mm x 8mm)
	IS62WV12816DALL-55BLI	mini BGA (6mm x 8mm), Lead-free
	IS62WV12816DALL-55B2I	mini BGA (6mm x 8mm), 2 CS Option

**ORDERING INFORMATION: IS62WV12816DBLL (2.5V - 3.6V)**

**Industrial Range: -40°C to +85°C**

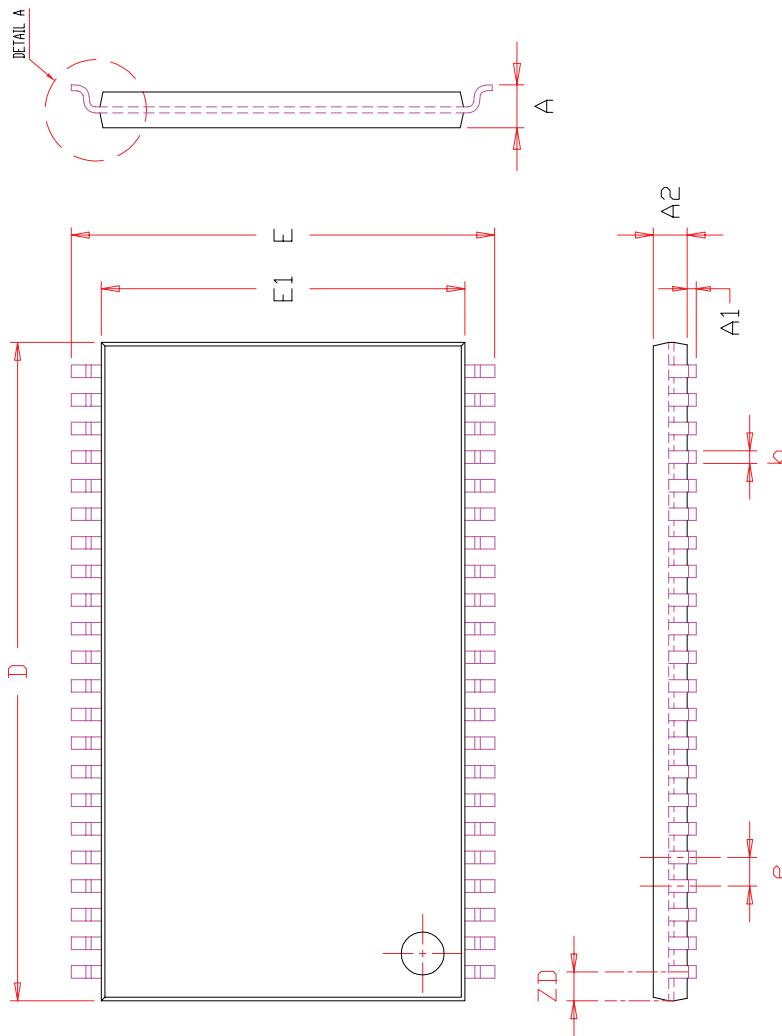
Speed (ns)	Order Part No.	Package
35	IS62WV12816DBLL-35TLI	TSOP (Type II), Lead-free
	IS62WV12816DBLL-35BLI	mini BGA (6mm x 8mm), Lead-free
	IS62WV12816DBLL-35B2LI	mini BGA (6mm x 8mm), 2 CS Option, Lead-free
45	IS62WV12816DBLL-45TLI	TSOP (Type II), Lead-free
	IS62WV12816DBLL-45BLI	mini BGA (6mm x 8mm), Lead-free
	IS62WV12816DBLL-45B2LI	mini BGA (6mm x 8mm), 2 CS Option, Lead-free
55	IS62WV12816DBLL-55TI	TSOP (Type II)
	IS62WV12816DBLL-55TLI	TSOP (Type II), Lead-free
	IS62WV12816DBLL-55BI	mini BGA (6mm x 8mm)
	IS62WV12816DBLL-55BLI	mini BGA (6mm x 8mm), Lead-free
	IS62WV12816DBLL-55B2I	mini BGA (6mm x 8mm), 2 CS Option
	IS62WV12816DBLL-55B2LI	mini BGA (6mm x 8mm), 2 CS Option, Lead-free

**ORDERING INFORMATION: IS65WV12816DBLL (2.5V - 3.6V)**

**Automotive Range (A3): -40°C to +125°C**

Speed (ns)	Order Part No.	Package
45	IS65WV12816DBLL-45TLA3	TSOP (Type II), Lead-free
	IS65WV12816DBLL-45BLA3	mini BGA (6mm x 8mm), Lead-free

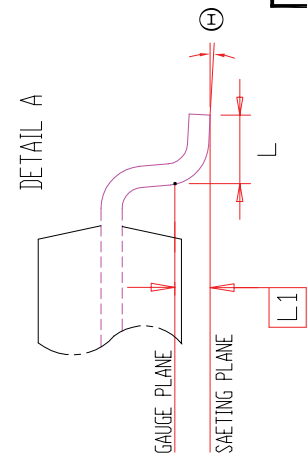




SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.45	0.012		0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40		0.69	0.016		0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
⊖	0		8°	0		8°

**NOTE :**

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



**TITLE**  
44L 400mil TSOP-2  
Package Outline

**REV.**  
F

**DATE**  
06/04/2008

06/04/2008